**CS219 Worksheet 2 (Ch4)**

Purpose: Become familiar with the MIPS architecture instruction formats, control signals, Datapath elements.

Points: 75

**Reading/References:** Chapter 4, Class Lecture / Lecture Notes, Textbook

1. Explain and trace/highlight the Datapath for the given R and I format instructions - **beq, ori, lw, sw,** Update the control signal table for each instruction. Rewrite the instruction using register format, for example change add into add rd, rs, rt. Use fig 4.17 for this question and you will need a separate picture for each instruction.

(Note: Use different color sketch/pen to easily identify the path of each instruction.) [40 pts, 10 pts each]

A diagram of a simple data path

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Table

Description automatically generated

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | RegDst  Mux | ALUSrc  Mux | MemtoReg  Mux | RegWrite | MemRead | MemWrite | Branch | Branch  Mux | ALUop1 (MSB) | Aluop0 (LSB) |
| beq |  |  |  |  |  |  |  |  |  |  |
| ori |  |  |  |  |  |  |  |  |  |  |
| lw |  |  |  |  |  |  |  |  |  |  |
| sw |  |  |  |  |  |  |  |  |  |  |

1. Explain and trace/highlight the Datapath for the given instructions:
2. j Label
3. ori rt, rs, imm

Use fig 4.24 for the above questions and you will need a separate picture for each instruction. (Note: Use different color sketch/pen to easily identify the path of each instruction.) [20 pts, 10 pts each]

A diagram of a jump system

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Note: This question(screenshot) is from textbook, however for the assignment we are considering a different diagram and values. I am sharing to let you know that, this is from textbook exercise and I have not changed any wording except numerical values. You no need to answer this sample(4.4, 4.4.1, 4.4.2,4.4.3)

Table

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1. In this problem(you have to calculate critical path), we examine how latencies of individual components of the Datapath affect the clock cycle time of the entire datapath, and how these components are utilized by instructions. For problems in this question, assume the following latencies for logic blocks in the datapath: [15 pts, 5 pts each]

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Processor** | **I-Mem** | **Add** | **Mux** | **ALU** | **Regs** | **D-Mem** | **Sign-Extend** | **Shift-Left- 2** |
| **A** | 300ns | 100ns | 30ns | 150ns | 80ns | 500ns | 20ns | 2ns |

1. If the only thing we need to do in a processor is fetch consecutive instructions (Figure 4.24), what would the cycle time be?
2. Consider a Datapath similar to the one in Figure 4.24, but for a processor that only has one type of instruction: unconditional branch instruction (b label == beq $0, $0, offset). What would the cycle time/critical path be for this Datapath?
3. Consider a Datapath similar to the one in Figure 4.24, but for a processor that only has one type of instruction: jump instruction (j Loop). What would the cycle time/critical path be for this Datapath?